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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,590	10/10/2003	Rama Divakaruni	FIS920030171	2589

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EXAMINER
TRAN, MAI HUONG C

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 07/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,590	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 June 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *1-11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/10/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

Application's election without traverse of Group I (Claims 12-20) drawn to a semiconductor device is acknowledged for prosecution in the subject application. Accordingly, claims 1-11 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Applicants have the right to file a divisional application covering the subject matter of the non-elected claims.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 12- are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent No. 6,262,450 to Kotecki et al.

Regarding to claim 12, Kotecki discloses an integrated circuit including a memory cell array and an external region outside of the memory cell array (col. 1, lines 35-39), comprising bitline contacts 54 to a substrate 34 and bitlines 52 disposed in the memory

cell array; and metallic conductive lines 46 interconnecting bitlines 52 to transistors 30 disposed in the external region, conductive lines 46 being patterned separately from the bitlines (col. 2, lines 59-67, cols. 3-4, and figs. 3-6a-b).

Regarding to claim 13, Kotecki discloses the integrated circuit wherein bitline contacts and bitlines are disposed in troughs formed in a dielectric region, each trough having a pair of vertical sidewalls, each sidewall extending substantially in a single plane between conductive lines and substrate (fig. 6a).

Regarding to claim 14, Kotecki discloses the integrated circuit further comprising conductive interconnections interconnecting bitlines to external transistors, conductive interconnections being patterned simultaneously with conductive lines (figs. 6a, 7).

Regarding to claim 15, Kotecki discloses the integrated circuit further comprising wordlines encapsulated by insulative material, wherein bitline contacts include borderless contacts disposed between encapsulated wordlines 12 (col. 2, lines 59-64, fig. 1).

Regarding to claim 16, Kotecki discloses the integrated circuit wherein bitline contacts include at least a first layer consisting essentially of polysilicon and bitlines include at least a second layer consisting essentially of at least one material selected from

the group consisting of metals and conductive compounds of metals (col. 3, lines 39-45, col. 4, lines 1-15).

Regarding to claim 17, Kotecki discloses the integrated circuit wherein bitlines and bitline contacts consist essentially of at least one material selected from the group consisting of metals and conductive compounds of metals (col. 4, lines 1-15).

Regarding to claim 18, Kotecki discloses the integrated circuit wherein conductive lines are broader than bitlines where conductive lines interconnect to bitlines (col. 3, lines 39-45).

Regarding to claim 19, Kotecki discloses the integrated circuit wherein conductive lines interconnect pairs of bitlines to sense amplifiers located in external regions beyond opposite edges of memory cell array, wherein successive pairs of bitlines are coupled to sense amplifiers located in alternating ones of external regions (col. 1, lines 30-39).

Regarding to claim 20, the integrated circuit wherein interconnections between conductive lines and bitlines are disposed over isolation structures, isolation structures isolating substrate from bitlines and conductive lines (col. 3, lines 47-53).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Mai-Huong Tran

David Nelms
Supervisory Patent Examiner
Technology Center 2800